What is claimed is:

1. A method of selecting a pattern to be measured comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point; and

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured

based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned.

2. The method of selecting a pattern to be measured according to claim 1,

wherein the fractional factorial design includes experimental arrangement based on an orthogonal array method.

3. The method of selecting a pattern to be measured according to claim 2,

wherein the orthogonal array method includes an orthogonal array method based on an L64 orthogonal array.

4. The method of selecting a pattern to be measured according to claim 1, further comprising:

defining second measurement points by further selecting some of the first measurement points.

5. A pattern inspection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further

selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned;

preparing a measurement schedule and actually executing measurement to the defined measurement points;

executing an analysis of variance from obtained measurement results on the basis of the fractional factorial design; and

changing the measurement schedule on the basis of the result of the analysis of variance.

6. The pattern inspection method according to claim 5, further comprising: bringing the result of the analysis of variance into view in the form of a table or a graph.

7. The pattern inspection method according to claim 5, further comprising: omitting some of the defined measurement points to define new measurement points on the basis of the result of the analysis of variance.

8. The pattern inspection method according to claim 5, wherein said some of the defined measurement points are omitted in use of a dummy method.

9. A pattern inspection method using a measurement device, said method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number

to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned; and

actually measuring a standard pattern prepared beforehand a predetermined times using the measurement device, prior to an actual measurement to the defined measurement point to evaluate reliability of the measurement device.

10. The pattern inspection method according to claim 9, further comprising: determining the number of measurements to the defined measurement points, when the result of evaluation of reliability of the measurement device is lower than a predetermined standard value, repeating the measurement to the measurement points by the determined number of measurements, and adopting an average value as a measured value of each measurement point.

11. A manufacturing method of a semiconductor device using a pattern inspection method, said pattern inspection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least

two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned;

preparing a measurement schedule and actually executing measurement to the defined measurement points;

executing an analysis of variance from obtained measurement results on the basis of the fractional factorial design; and

changing the measurement schedule on the basis of the result of the analysis of variance.

12. The manufacturing method of a semiconductor device according to claim 11,

wherein said pattern inspection method further

comprising:

preparing a measurement schedule and actually executing measurement to the defined measurement points;

executing an analysis of variance from obtained measurement results on the basis of the fractional factorial design; and

changing the measurement schedule on the basis of the result of the analysis of variance.

13. A program which allows a computer to implement a method of selecting a pattern to be measured, said selection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four

lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point; and

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned.

14. A program which allows a computer to implement a pattern inspection method, said pattern inspection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected

semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned;

preparing a measurement schedule and actually executing measurement to the defined measurement points;

executing an analysis of variance from obtained measurement results on the basis of the fractional factorial design; and

changing the measurement schedule on the basis of the result of the analysis of variance.

15. A pattern inspection apparatus which is capable to communicate with an external inspection device and which prepares a schedule to measure a pattern to supply the prepared measurement schedule to the external inspection device, said pattern inspection apparatus comprising:

a controller which receives information of a measurement point defined as a point to be actually measured to prepare a measurement schedule and supplies a first command signal to execute measurement to the defined measurement point to the external inspection device, the measurement point being defined by:

assigning first wafer numbers in order of a process

with respect to a wafer group constituted of a plurality of wafers including semiconductor chip groups in which patterns are formed by a fine processing process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two or more wafers having serial first wafer numbers from the first sub-group to assign second wafer numbers;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-group, further selecting a chip including the center position of the wafer inside if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions exceeding a quantity of at least two rows and two columns based on in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points in the pattern formed on the wafer as only one candidate measurement point with respect to the lattice point, and assigning a candidate measurement point number to the candidate measurement point; and

selecting only some of the candidate measurement points to which the candidate measurement point numbers have been assigned based on a fractional factorial design with respect to the respective semiconductor chips to which the chip numbers have been assigned.

16. The pattern inspection apparatus according to claim 15, further comprising:

a calculator which receives information of a

measurement result from the external inspection device, and executes an analysis of variance on the basis of the fractional factorial design,

wherein the controller changes the measurement schedule on the basis of the result of the analysis of variance and transmits a second command signal to execute measurement in accordance with the changed measurement schedule to the external inspection device.

17. The pattern inspection apparatus according to claim 16,

wherein the controller omits some of the defined measurement points on the basis of the result of the analysis of variance and defines new measurement points to change the measurement schedule.

18. The pattern inspection apparatus according to claim 15,

wherein the controller transmits a third command signal to the external inspection device to measure a standard pattern prepared beforehand a predetermined times, prior to the transmission of the first command signal, and evaluates reliability of the external measurement device on the basis of the measurement result supplied from the external inspection device.

19. The pattern inspection apparatus according to claim 18,

wherein the controller determines the number of times of measurement to the measurement points, when the result of the evaluation of the reliability of the external measurement device is lower than a predetermined standard value, produces and transmits a fourth command signal to the external inspection device to repeat the measurement to the measurement points the determined number of measurement times, and adopts an average value of the measurement results from the external inspection device which has executed inspection in response to the fourth command signal as a measured value of each measurement point.

20. The pattern inspection apparatus according to claim 15, further comprising:

a terminal device which receives information of the result of the analysis of variance from the controller to process the information into visible information of a table or a graph; and

a display which displays the information of the table or the graph.